Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DAVID C. REYNOLDS

Appeal No. 1998-3024
Application No. 08/464,298

ON BRIEF

Before HAIRSTON, HECKER, and DIXON, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

## DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 8. In an Amendment After Final (paper number 8), claims 1 through 3, 5, 6 and 8 were canceled, and claims 4 and 7 were amended. Accordingly, claims 4 and 7 remain before us on appeal.

The disclosed invention relates to a CMOS distribution system and method.

Claim 4 is illustrative of the claimed invention, and it reads as follows:

4. A CMOS distribution system with means for efficiently merging two synchronized data signals comprising:

a first clocked CMOS signal source having an output;

first clock means producing first clock pulses and coupled to said first signal source to activate said first signal source at the times of occurrence of said first clock pulses;

a second clocked CMOS signal source and having an output synchronized with the output of said first clocked CMOS signal source;

second clock means producing second clock pulses synchronized with and occurring at times complementary to said first clock pulses;

means coupling said second clock pulses to said second signal source to activate said second signal source at the times of occurrence of said second clock pulses;

first and second transmission gates having inputs and outputs with the inputs coupled to the outputs of said first and second signal sources respectively;

first phase-shifting means coupled to said first clock means to produce third clock pulses phase-shifted by at least approximately 90°;

means to couple said third clock pulses to said first transmission gate to activate said first gate at the times of occurrence of said third clock pulses;

second phase-shifting means coupled to said second clock means to produce fourth clock pulses phase-shifted by at least approximately 90°;

means to couple said fourth clock pulses to said second transmission gate to activate said second gate at the times of occurrence of said fourth clock pulses;

and

means to couple together the outputs of said first and second transmission gates to form a multiplexer for merging the signals produced at the outputs of said first and second transmission gates to develop a stream of signals corresponding to a composite of said synchronized output signals from said first and second clocked CMOS signal sources.

The reference relied on by the examiner is:

Archer et al. (Archer) 3,947,697 Mar. 30, 1976

Claims 4 and 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over the prior art Figure 1 of the instant application in view of Archer.

Reference is made to the briefs and the answers for the respective positions of the appellant and the examiner.

OPINION

The obviousness rejection of claims 4 and 7 is reversed.

According to the examiner (Answer, page 4), "the prior art Fig. 1 fails to show that the clock signals provided to the gates 18 and 20 are delayed signals of the clock signals to the first and second signal sources 10-12 as required by claims 4 and 7." For such a teaching, the examiner turns to Archer which "teaches in Fig. 1 that a clock signal to a signal source B can be provided to a transmission gate 3 after a certain delay to protect 'against the flip-flops synchronizing in an unstable state due to the critical period of the sampling edge of the clock pulse'" (Answer, page 4). In view of the teachings of Archer, the examiner concludes that it would have been obvious to the skilled artisan "to use the delay circuit T of Archer at the output of each clock means 14 and 16 of the prior art Fig. 1 in order to delay each output to thereby protect 'against the flip-flops synchronizing in an unstable state' and enable 'the output information of the flip-flop only after a time T after which the probability of being in an unstable state is acceptable'" (Answer, page 5).

Appellant argues inter alia that claims 4 and 7 recite "first and second phase-shifting means to develop phase-

shifted clock pulses for the two alternately-activated transmission gates respectively" to introduce phase shifts of approximately 90 degrees, and that "[s]ubstitution of Archer's 'delay circuit T' between clock sources 14, 16 and the respective transmission gates 18, 20 would not meet that recital of Claim 4 because that delay circuit produces a fixed time delay" (Brief, page 6).

In rebuttal, the examiner states (Answer, page 5) that "the claimed first and second phase shifting means are disclosed by the combination of the prior art Fig. 1 and the Archer reference in that a delay is coupled to each gate output of the two clock means 14 and 16 so as to constitute first and second phase shifting means."

Notwithstanding the time delay clocking teachings of Archer, we agree with appellant (Reply Brief, page 2) that:

> Use of phase-shifting means assures that the signal source clock pulses are separated in time from the multiplexer clock pulses by a fixed number of degrees of the clock cycle (specifically, one-quarter of a CLK/2 cycle), not by a fixed time period as in Archer. In applicant's invention, the time duration between the signal source clock pulses and the multiplexer clock pulses will necessarily change with changes in clock frequency (e.g., decreasing duration with increasing frequency).

In view of this distinction between Archer and the claimed invention, we will reverse the obviousness rejection of claims 4 and 7.

DECISION

The decision of the examiner rejecting claims 4 and 7 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON )
Administrative Patent Judge )
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) BOARD OF PATENT
STUART N. HECKER ) APPEALS

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| Administrative Patent Judge | ) | AND |
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| JOSEPH L. DIXON | ) | |
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Appeal No. 1998-3024
Application No. 08/464,298

APJ HAIRSTON

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DECISION: REVERSED
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s):
Prepared: May 17, 2002

Draft Final

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PALM / ACTS 2 / BOOK
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